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| **LESSON PLAN** | | | | | |
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| Discipline | | | COMPUTER ENGG. | | |
| Semester | | | 4th | | |
| Subject | | | MPI | | |
| Lesson Plan Duration : | | | 15 Weeks ( From March 2022 to June 2020 ) | | |
| Work Load (Lecture/Practical) per Week (in Hours) : **Lecture – 03 , Practical - 03** | | | | | |
| Week |  | **Theory** | | **Practical** | |
| Lecture | Topic | | Practical | Topic |
| Day | (including assignment/test ) | | Day |
| Ist | 1 | **1.Evolution of Microprocessor :** Typical organization of a microcomputer system and functions of its various blocks | | 1 | Familiarization of different keys of 8085 microprocessor kit and its memory map |
| 2 | Microprocessor its evolution, function | | 2 |
| 3 | Impact on modern society | | 3 |
| 4 | **2. Architecture of a Microprocessor** | | 4 |
| 2nd | 5 | Concept of Bus, bus organization of 8085 | | 5 | Familiarization of different keys of 8085 microprocessor kit and its memory map |
| 6 | Functional block diagram of 8085 | | 6 |
| 7 | Pin details of 8085 and related signals | | 7 |
| 8 | Demultiplexing of address / data bus | | 8 |
| 3rd | 9 | Generation of read/ write control signals | | 9 | Steps to enter modify data/ program and to execute a programme on 8085 kit |
| 10 | Steps to execute a stored programme | | 10 |
| 11 | 3. **Instruction Timing and Cycles** : | | 11 |
| 12 | Instruction cycle | | 12 |
| 4th | 13 | Machine cycle and T-states | | 13 | Writing and execution of ALP for addition and sub station of two 8 bit numbers. |
| Fetch and execute cycle | |
| 14 | Brief idea of machine and assembly languages | | 14 |
| 15 | Machines and Mnemonic codes. | | 15 |
| 16 | Addressing mode | | 16 |
| 5th | 17 | Identification of instructions as to which addressing mode they belong | | 17 | Writing and execution of ALP for addition and sub station of two 8 bit numbers. |
| 18 | Concept of Instruction set | | 18 |
| 19 | Explanation of the instructions of the following group of instruction set. | | 19 |
| 20 | Data transfer group | | 20 |
| 6th | 21 | Logic group | | 21 | Writing and execution of ALP for multiplication and division of two 8 bit Number |
| 22 | I/O Control Group | | 22 |
| 23 | Machine Control Group | | 23 |
| 24 | Programming exercises in assembly language | | 24 |
| 7th | 25 | Programming exercises in assembly  language | | 25 | Writing and execution of ALP for multiplication and division of two 8 bit  Number |
| 26 | Programming exercises in assembly language | | 26 |

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|  | 27 | Programming exercises in assembly language | 27 |  |
| 28 | Programming exercises in assembly  language | 28 |
| 8th | 29 | 5**. Memories and I/O Interfacing:**  Address decoding, | 29 | Writing and execution of ALP for arranging 10 number in ascending/ descending order |
| 30 | Address decoding | 30 |
| 31 | Address decoding | 31 |
| 32 | Concept of peripheral mapped I/O and memory mapped I/O | 32 |
| 9th | 33 | Concept of peripheral mapped I/O and  memory mapped I/O | 33 | Writing and execution of ALP for arranging 10 number in ascending/ descending order |
| 34 | Concept of peripheral mapped I/O and memory mapped I/O | 34 |
| 35 | Concept of peripheral mapped I/O and  memory mapped I/O | 35 |
| 36 | Interfacing of memory mapped I/O devices | 36 |
| 10th | 37 | Interfacing of memory mapped I/O  devices | 37 | Writing and execution of ALP for 0 to 9 BCD counters ( up/down counteraccording to choice stored in memory  ) |
| 38 | **6. Interrupts : Maskable and non- maskable** | 38 |
| 39 | Maskable and non-maskable | 39 |
| 40 | Maskable and non-maskable | 40 |
| 11th | 41 | Software Interrupt | 41 | Writing and execution of ALP for 0 to 9 BCD counters ( up/down counteraccording to choice stored in memory  ) |
| 42 | Software Interrupt | 42 |
| 43 | Various hardware interrupts | 43 |
| 44 | Various hardware interrupts | 44 |
| 12th | 45 | Various hardware interrupts | 45 | Interfacing exercise on 8255 like LED display control |
| 46 | Servicing interrupts | 46 |
| 47 | Servicing interrupts | 47 |
| 48 | 7. **Data Transfer Techniques** :Concept of Programmed I/O operations | 48 |
| 13th | 49 | Concept of Programmed I/O operations | 49 | Interfacing exercise on 8253 programmable interval timer |
| 50 | Concept of Programmed I/O operations | 50 |
| 51 | Sync Data Transfer | 51 |
| 52 | Async data transfer( hand shaking ) | 52 |
| 14th | 53 | DMA | 53 | interfacing exexercise on 8279 programmable KB/ display interface like to display the hex code of key pressed on display |
| 54 | DMA | 54 |
| 55 | 8. **Peripheral devices**: 8255 PPI | 55 |
| 56 | 8257 DMA | 56 |
| 15th | 57 | Controller | 57 | Use of 8085 emulator for hardware testing |
| 58 | 9. **Architecture of 8086 Microprocessor** : Block diagram | 58 |
| 59 | Minimum and maximum mode | 59 |
| 60 | Pin and Signals | 60 |